IN THE CLAIMS

Please cancel claims 1-18.

Please add the following new claims 23-38 as set forth below:

23. (New) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said second layer comprises a metal.

24. (New) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said second layer comprises a refractive metal.

25. (New) A semiconductor device substantially impervious to the effects of buckling, according to claim 19, wherein said second layer comprises at least one of boroposphosilicate glass ("BPGS") and tetraethylorthosilicate ("TEOS").

26. (New) A planar multilayered semiconductor device comprising:

a first flowable layer having a thermal coefficient of expansion;

a nitride film superjacent said first layer; and

another flowable layer superjacent said film, said another flowable layer having another thermal coefficient of expansion.

27. (New) The planar multilayered semiconductor device according to claim 26, wherein said nitride film isolates said first flowable layer from said another flowable layer, thereby preventing said first flowable layer and said another flowable layer from interacting when heated.

28. (New) The planar multilayered semiconductor device according to claim 27, wherein said first flowable layer and said another flowable layer reflow at a temperature of at least 700°C.

29. (New) The planar multilayered semiconductor device according to claim 28, wherein said nitride film comprises at least one of titanium nitride, tantalum nitride, and silicon nitride.

30. (New) The planar multilayered semiconductor device according to claim 29, wherein said first flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

31. (New) The planar multilayered semiconductor device according to claim 30, wherein said first flowable layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

32. (New) The planar multilayered semiconductor device according to claim 30, wherein said first flowable layer comprises at least one of single crystal silicon, polycrystalline silicon, amorphous silicon.

33. (New) A multilayer heterostructure semiconductor device having a planar configuration comprising:

a semiconductor substrate;

a planarization layer disposed superjacent said substrate, said planarization layer having a first thermal coefficient of expansion;

a barrier film disposed superjacent said planarization layer, said barrier film having structural integrity; and

another layer disposed superjacent said barrier film, said barrier film for preventing said planarization layer and said another layer from interacting when heated, said another layer having a second thermal coefficient of expansion.

34. (New) The multilayered heterostructure semiconductor device according to claim 33, wherein said barrier film comprises at least one of titanium nitride, tantalum nitride, titanium oxide, silicon nitride, tantalum oxide, silicon dioxide, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

35. (New) The multilayered heterostructure semiconductor device according to claim 34, wherein said planarization layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, single crystal silicon, polycrystalline silicon, amorphous silicon, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

36. (New) The multilayered heterostructure semiconductor device according to claim 35, wherein said another layer comprises at least one of tungsten, titanium, tantalum, copper, aluminum, borophosphosilicate glass ("BPSG") and tetraethylorthosilicate ("TEOS").

37. (New) The multilayered heterostructure semiconductor device according to claim 33, wherein said planarization layer and said another layer reflow at a temperature of at least 700°C.

38. (New) The multilayered heterostructure semiconductor device according to claim 37, wherein said structural integrity of said barrier layer is maintained when heated to a temperature of at least 700°C.